

# DATA SHEET



## **PCA9548** 8-channel I<sup>2</sup>C switch with reset

Product data sheet  
Supersedes data of 2002 Feb 19

2004 Sep 30

8-channel I<sup>2</sup>C switch with reset

PCA9548



## FEATURES

- 1-of-8 bi-directional translating switches
- I<sup>2</sup>C interface logic; compatible with SMBus standards
- Active LOW Reset Input
- 3 address pins allowing up to 8 devices on the I<sup>2</sup>C-bus
- Channel selection via I<sup>2</sup>C-bus, in any combination
- Power-up with all switch channels deselected
- Low R<sub>dsON</sub> switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant Inputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V per JESD22-C101
- Latchup testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO24, TSSOP24

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic SO	-40 °C to +85 °C	PCA9548D	SOT137-1
24-Pin Plastic TSSOP	-40 °C to +85 °C	PCA9548PW	SOT355-1

Standard packing quantities and other packaging data are available at [www.standardproducts.philips.com/packaging](http://www.standardproducts.philips.com/packaging).

## DESCRIPTION

The PCA9548 is a octal bi-directional translating switch controlled by the I<sup>2</sup>C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable Control Register.

An active-LOW reset input allows the PCA9548 to recover from a situation where one of the downstream I<sup>2</sup>C-buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I<sup>2</sup>C state machine and causes all the channels to be deselected as does the internal power on reset function.

The pass gates of the switches are constructed such that the V<sub>DD</sub> pin can be used to limit the maximum high voltage which will be passed by the PCA9548. This allows the use of different bus voltages on each pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

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## PIN CONFIGURATION — SO, TSSOP

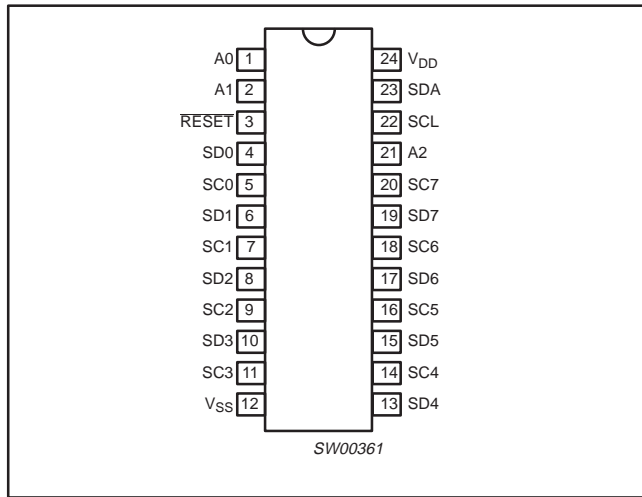


Figure 1. Pin configuration — SO, TSSOP

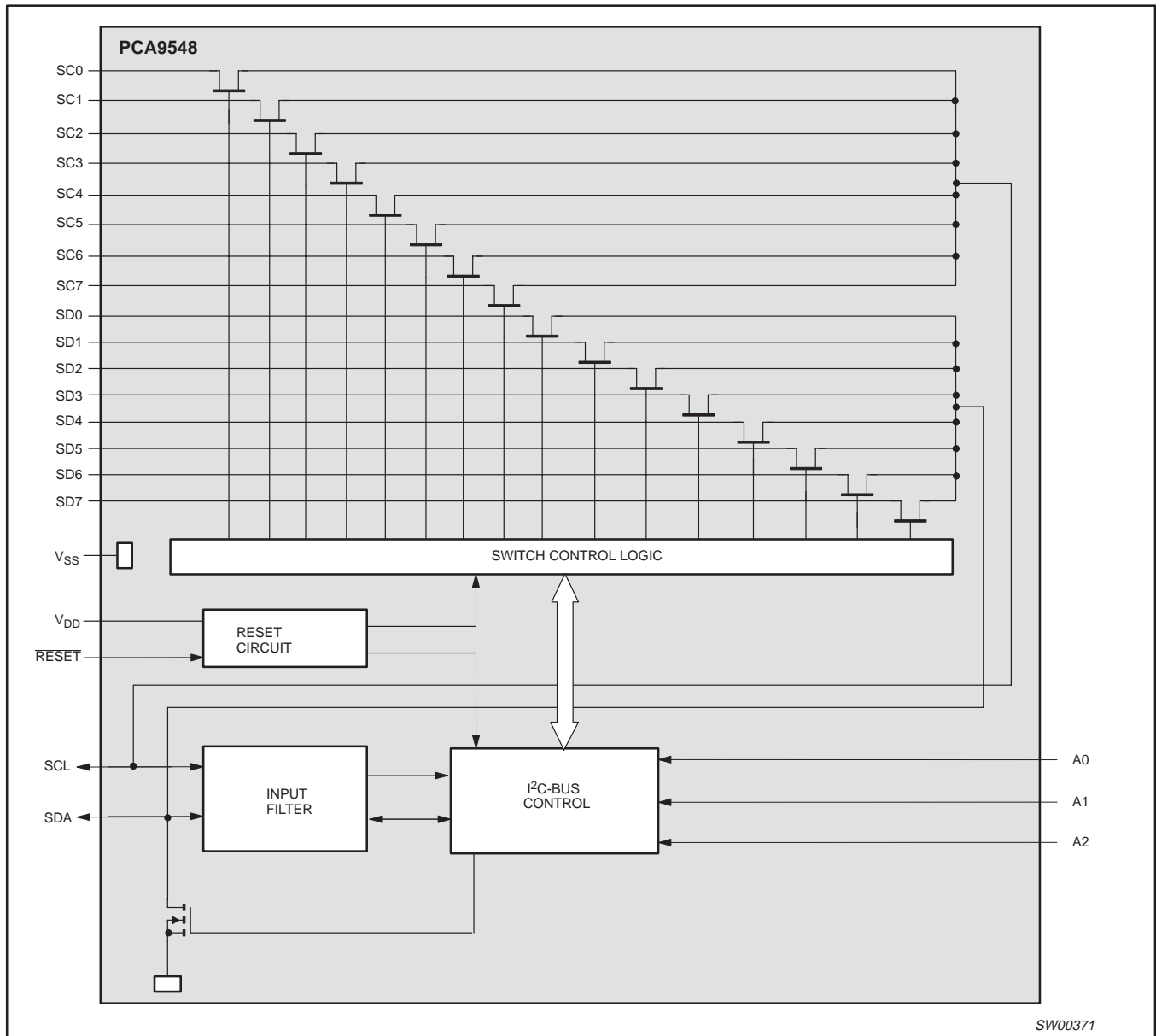
## PIN DESCRIPTION

SO, TSSOP PIN NUMBER	SYMBOL	FUNCTION
1	A0	Address input 0
2	A1	Address input 1
3	RESET	Active LOW reset input
4	SD0	Serial data output 0
5	SC0	Serial clock output 1
6	SD1	Serial data output 1
7	SC1	Serial clock output 2
8	SD2	Serial data output 2
9	SC2	Serial clock output 3
10	SD3	Serial data output 3
11	SC3	Serial clock output 4
12	V <sub>SS</sub>	Supply ground
13	SD4	Serial data output 4
14	SC4	Serial clock output 5
15	SD5	Serial data output 5
16	SC5	Serial clock output 6
17	SD6	Serial data output 6
18	SC6	Serial clock output 7
19	SD7	Serial data output 7
20	SC7	Serial clock output 8
21	A2	Address input 2
22	SCL	Serial clock line
23	SDA	Serial data line
24	V <sub>DD</sub>	Supply voltage

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## BLOCK DIAGRAM



SW00371

Figure 2. Block diagram

# 8-channel I<sup>2</sup>C switch with reset

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## DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9548 is shown in Figure 3. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

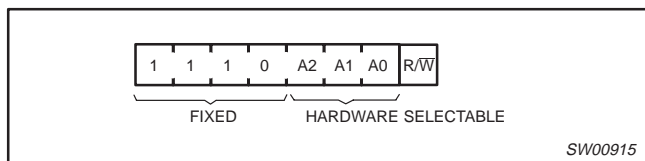


Figure 3. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

## CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9548, which will be stored in the control register. If multiple bytes are received by the PCA9548, it will save the last byte received. This register can be written and read via the I<sup>2</sup>C-bus.

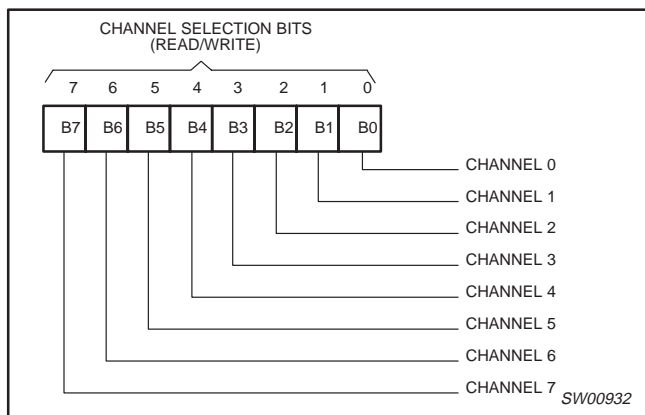


Figure 4. Control register

## CONTROL REGISTER DEFINITION

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9548 has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a stop condition has been placed on the I<sup>2</sup>C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 1. Control Register; Write — Channel Selection/  
Read — Channel Status

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND	
X	X	X	X	X	X	X	0	Channel 0 disabled	
							1	Channel 0 enabled	
X	X	X	X	X	X	X	0	Channel 1 disabled	
							1	Channel 1 enabled	
X	X	X	X	X	0	X	X	0	Channel 2 disabled
								1	Channel 2 enabled
X	X	X	X	0	X	X	X	0	Channel 3 disabled
								1	Channel 3 enabled
X	X	X	0	X	X	X	X	0	Channel 4 disabled
								1	Channel 4 enabled
X	X	0	X	X	X	X	X	0	Channel 5 disabled
								1	Channel 5 enabled
X	0	X	X	X	X	X	X	0	Channel 6 disabled
								1	Channel 6 enabled
0	X	X	X	X	X	X	X	0	Channel 7 disabled
								1	Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state	

**NOTE:** Several channels can be enabled at the same time.  
Ex: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that channels 7, 5, 4, 1, and 0 are disabled and channels 6, 3, and 2 are enabled.  
Care should be taken not to exceed the maximum bus capacitance.

## RESET INPUT

The RESET input is an active-LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of t<sub>VL</sub>, the PCA9548 will reset its registers and I<sup>2</sup>C state machine and will deselect all channels. The RESET input must be connected to V<sub>DD</sub> through a pull-up resistor.

## POWER-ON RESET

When power is applied to V<sub>DD</sub>, an internal Power On Reset holds the PCA9548 in a reset state until V<sub>DD</sub> has reached V<sub>POR</sub>. At this point, the reset condition is released and the PCA9548 registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes causing all the channels to be deselected.

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## VOLTAGE TRANSLATION

The pass gate transistors of the PCA9548 are constructed such that the V<sub>DD</sub> voltage can be used to limit the maximum voltage that will be passed from one I<sup>2</sup>C-bus to another.

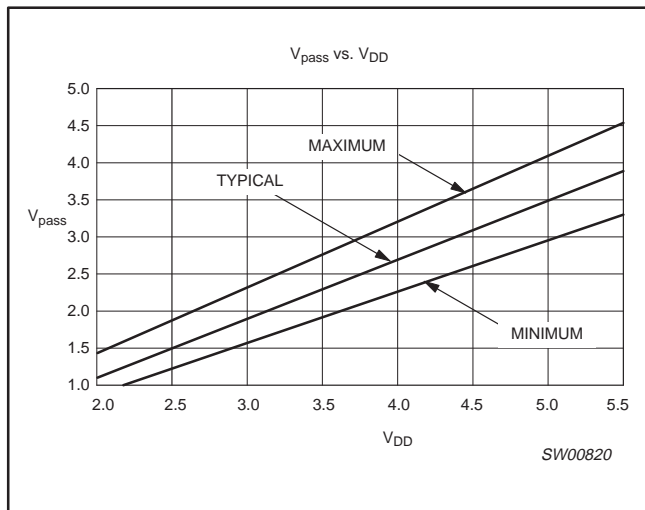


Figure 5. V<sub>pass</sub> voltage vs. V<sub>DD</sub>

Figure 5 shows the voltage characteristics of the pass gate transistors (note that the PCA9548 is only tested at the points specified in the DC Characteristics section of this datasheet). In order for the PCA9548 to act as a voltage translator, the V<sub>pass</sub> voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then V<sub>pass</sub> should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 5, we see that V<sub>pass</sub> (max.) will be at 2.7 V when the PCA9548 supply voltage is 3.5 V or lower so the PCA9548 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 12).

More Information can be found in Application Note AN262 *PCA954X family of I<sup>2</sup>C/SMBus multiplexers and switches*.

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### CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

#### Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

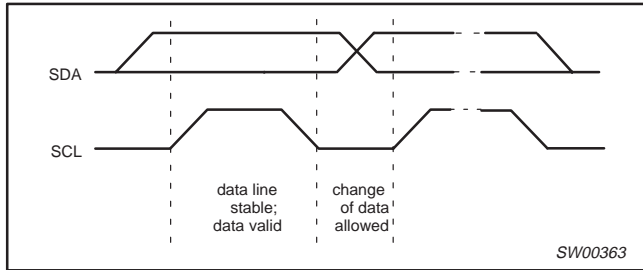


Figure 6. Bit transfer

#### Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

#### System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 8).

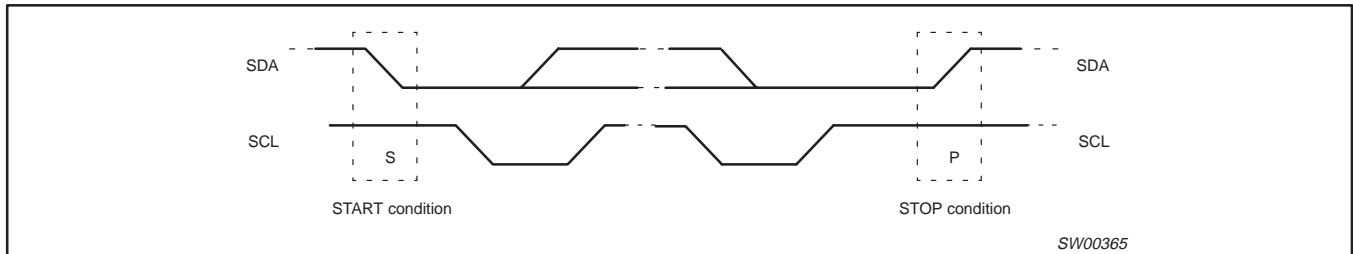


Figure 7. Definition of start and stop conditions

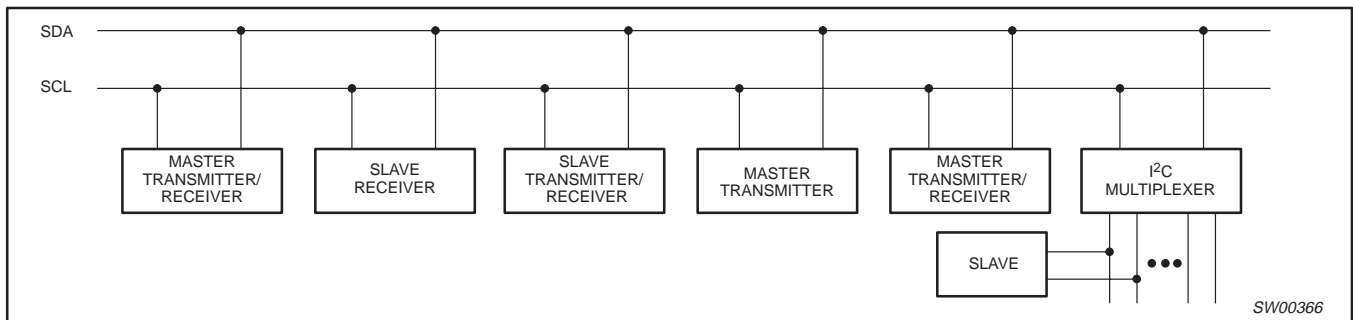


Figure 8. System configuration

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## Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

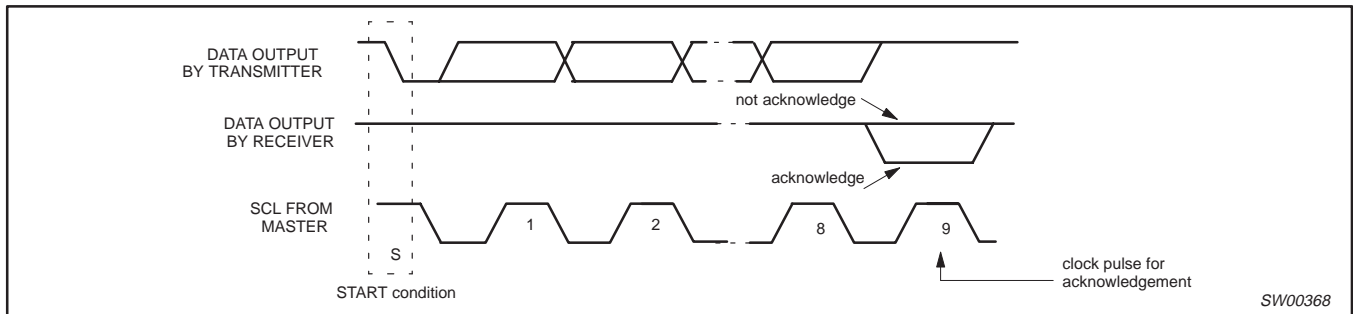


Figure 9. Acknowledgement on the I<sup>2</sup>C-bus

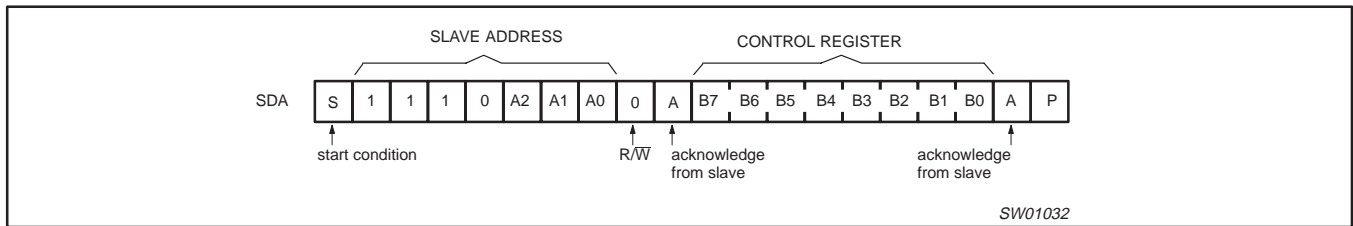


Figure 10. WRITE control register

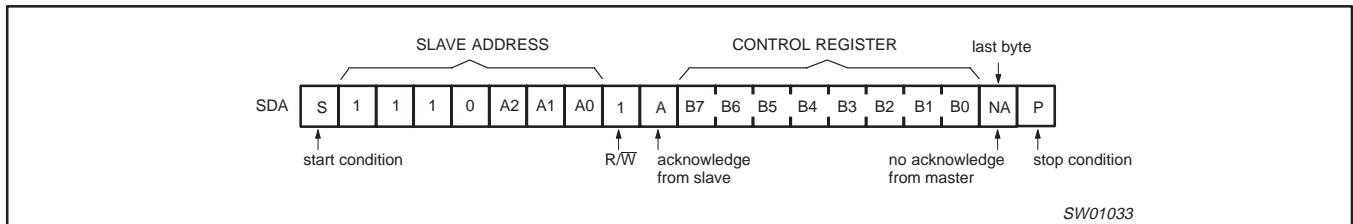


Figure 11. READ control register



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## TYPICAL APPLICATION

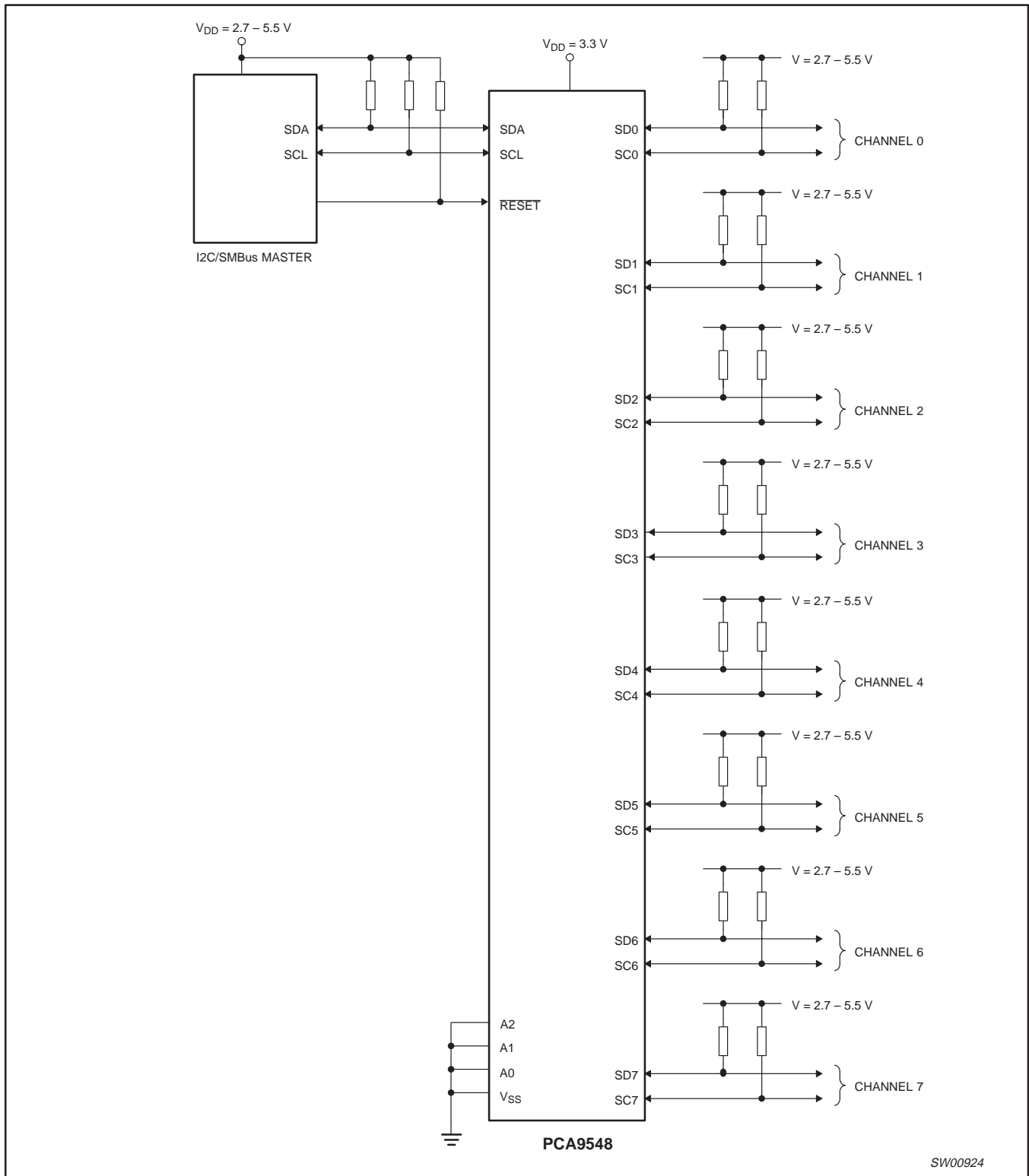


Figure 12. Typical application

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>DD</sub>	DC supply voltage		-0.5 to +7.0	V
V <sub>I</sub>	DC input voltage		-0.5 to +7.0	V
I <sub>I</sub>	DC input current		±20	mA
I <sub>O</sub>	DC output current		±25	mA
I <sub>DD</sub>	Supply current		±100	mA
I <sub>SS</sub>	Supply current		±100	mA
P <sub>tot</sub>	total power dissipation		400	mW
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C
T <sub>amb</sub>	Operating ambient temperature		-40 to +85	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

**DC CHARACTERISTICS**V<sub>DD</sub> = 2.3 V to 3.6 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. (See page 11 for V<sub>DD</sub> = 3.6 V to 5.5 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>Supply</b>						
V <sub>DD</sub>	Supply voltage		2.3	—	3.6	V
I <sub>DD</sub>	Supply current	Operating mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	—	45	100	μA
I <sub>stb</sub>	Standby current	Standby mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	25	100	μA
V <sub>POR</sub>	Power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	1.6	2.1	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	—	0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	—	6	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	—	—	mA
		V <sub>OL</sub> = 0.6 V	6	—	—	
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	—	+1	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	20	21	pF
<b>Select inputs A0 to A2 / RESET</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	—	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	—	V <sub>DD</sub> + 0.5	V
I <sub>LI</sub>	Input leakage current	pin at V <sub>DD</sub> or V <sub>SS</sub>	-1	—	+1	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	2	5	pF
<b>Pass Gate</b>						
R <sub>ON</sub>	Switch resistance	V <sub>CC</sub> = 3.67 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 15 mA	5	20	30	Ω
		V <sub>CC</sub> = 2.3 V to 2.7 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 10 mA	7	26	55	
V <sub>Pass</sub>	Switch output voltage	V <sub>swin</sub> = V <sub>DD</sub> = 3.3 V; I <sub>swout</sub> = -100 μA	—	2.2	—	V
		V <sub>swin</sub> = V <sub>DD</sub> = 3.0 V to 3.6 V; I <sub>swout</sub> = -100 μA	1.6	—	2.8	
		V <sub>swin</sub> = V <sub>DD</sub> = 2.5 V; I <sub>swout</sub> = -100 μA	—	1.5	—	
		V <sub>swin</sub> = V <sub>DD</sub> = 2.3 V to 2.7 V; I <sub>swout</sub> = -100 μA	1.1	—	2.0	
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	—	+1	μA
C <sub>io</sub>	Input/output capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	3	5	pF

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**DC CHARACTERISTICS**V<sub>DD</sub> = 3.6 V to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. (See page 10 for V<sub>DD</sub> = 2.3 V to 3.6 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>Supply</b>						
V <sub>DD</sub>	Supply voltage		3.6	—	5.5	V
I <sub>DD</sub>	Supply current	Operating mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	—	575	600	μA
I <sub>stb</sub>	Standby current	Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	250	300	μA
V <sub>POR</sub>	Power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	1.7	2.1	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	—	0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	—	6	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	—	—	mA
		V <sub>OL</sub> = 0.6 V	6	—	—	mA
I <sub>IL</sub>	LOW-level input current	V <sub>I</sub> = V <sub>SS</sub>	-10	—	+10	μA
I <sub>IH</sub>	HIGH-level input current	V <sub>I</sub> = V <sub>DD</sub>	—	—	100	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	20	21	pF
<b>Select inputs A0 to A2 / RESET</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	—	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	—	V <sub>DD</sub> + 0.5	V
I <sub>LI</sub>	Input leakage current	pin at V <sub>DD</sub> or V <sub>SS</sub>	-1	—	+50	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	2	5	pF
<b>Pass Gate</b>						
R <sub>ON</sub>	Switch resistance	V <sub>CC</sub> = 4.5 V to 5.5 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 15 mA	4	11	24	Ω
V <sub>Pass</sub>	Switch output voltage	V <sub>swin</sub> = V <sub>DD</sub> = 5.0 V; I <sub>swout</sub> = -100 μA	—	3.5	—	V
		V <sub>swin</sub> = V <sub>DD</sub> = 4.5 V to 5.5 V; I <sub>swout</sub> = -100 μA	2.6	—	4.5	V
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-10	—	+10	μA
C <sub>io</sub>	Input/output capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	3	5	pF

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## AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD-MODE I <sup>2</sup> C-BUS		FAST-MODE I <sup>2</sup> C-BUS		UNIT
		MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Propagation delay from SDA to SD <sub>n</sub> or SCL to SC <sub>n</sub>	—	0.3 <sup>1</sup>	—	0.3 <sup>1</sup>	ns
f <sub>SCL</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
t <sub>HD;STA</sub>	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7	—	1.3	—	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t <sub>SU;STA</sub>	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t <sub>SU;STO</sub>	Set-up time for STOP condition	4.0	—	0.6	—	μs
t <sub>HD;DAT</sub>	Data hold time	0 <sup>2</sup>	3.45	0 <sup>2</sup>	0.9	μs
t <sub>SU;DAT</sub>	Data set-up time	250	—	100	—	ns
t <sub>R</sub>	Rise time of both SDA and SCL signals	—	1000	20 + 0.1C <sub>b</sub> <sup>3</sup>	300	ns
t <sub>F</sub>	Fall time of both SDA and SCL signals	—	300	20 + 0.1C <sub>b</sub> <sup>3</sup>	300	μs
C <sub>b</sub>	Capacitive load for each bus line	—	400	—	400	μs
t <sub>SP</sub>	Pulse width of spikes which must be suppressed by the input filter	—	50	—	50	ns
t <sub>VD;DATL</sub>	Data valid (HL)	—	1	—	1	μs
t <sub>VD;DATH</sub>	Data valid (LH)	—	0.6	—	0.6	μs
t <sub>VD;ACK</sub>	Data valid Acknowledge	—	1	—	1	μs
<b>RESET</b>						
t <sub>WL(rst)</sub>	Pulse width low reset	4	—	4	—	ns
t <sub>rst</sub>	Reset time (SDA clear)	500	—	500	—	ns
t <sub>REC;STA</sub>	Recovery to Start	0	—	0	—	ns

**NOTES:**

1. Pass gate propagation delay is calculated from the 20 Ω typical R<sub>ON</sub> and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH(min)</sub> of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. C<sub>b</sub> = total capacitance of one bus line in pF.

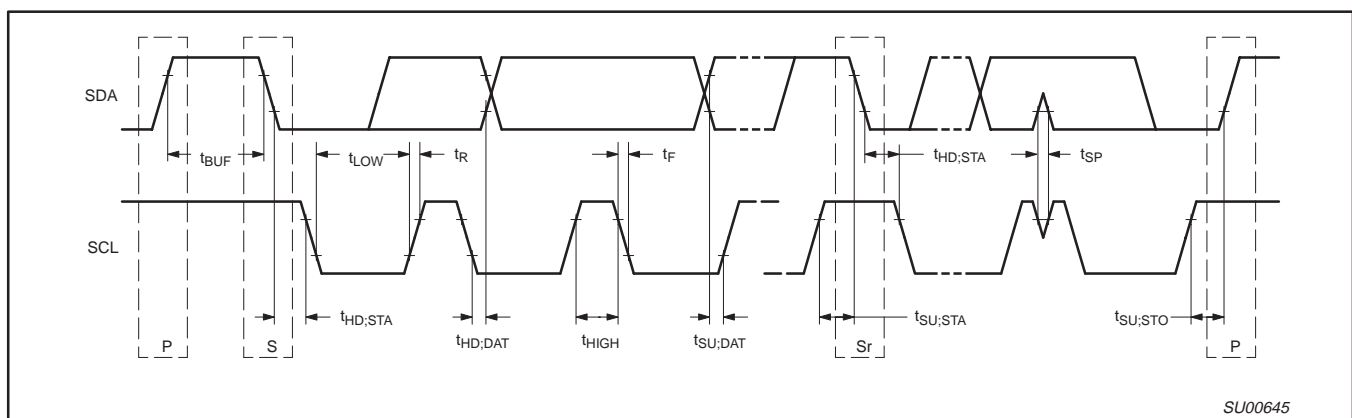


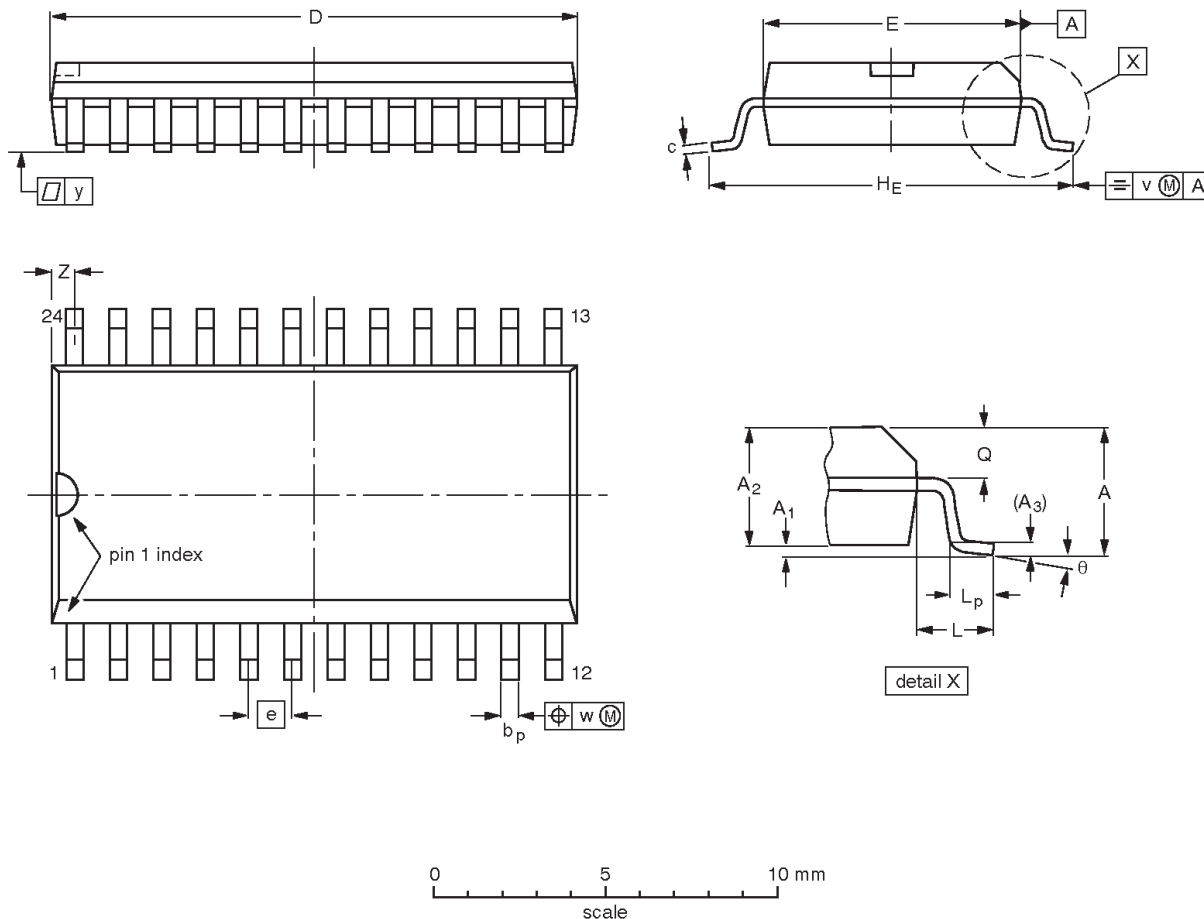
Figure 13. Definition of timing on the I<sup>2</sup>C-bus

# 8-channel I<sup>2</sup>C switch with reset

PCA9548

**SO24:** plastic small outline package; 24 leads; body width 7.5 mm

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

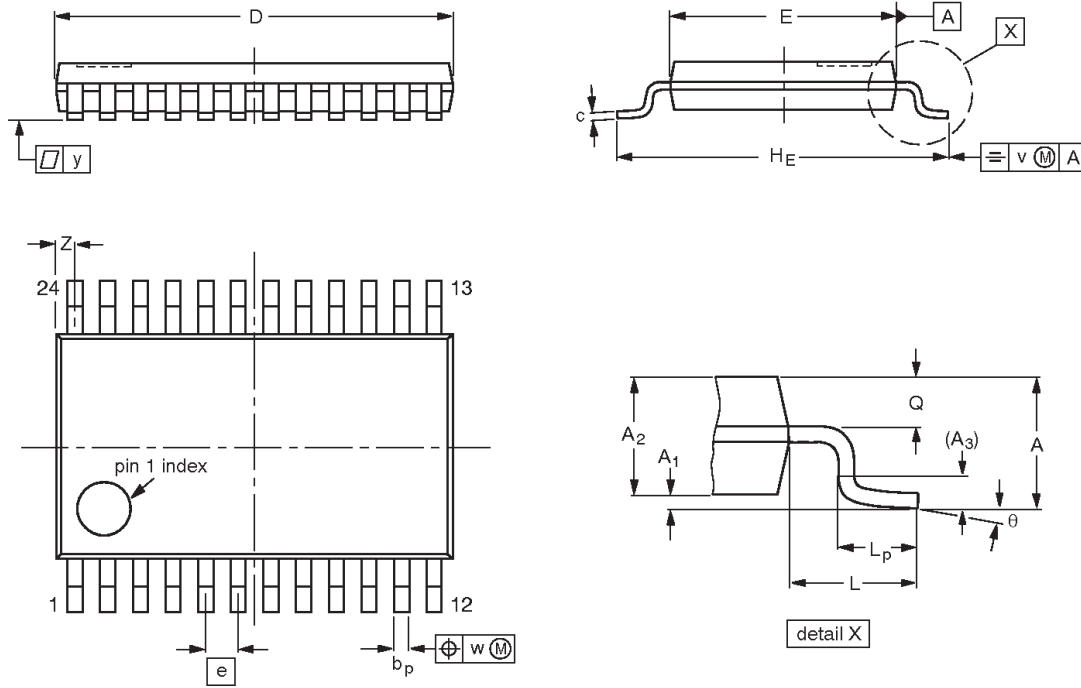
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				-99-12-27 03-02-19

# 8-channel I<sup>2</sup>C switch with reset

PCA9548

**TSSOP24:** plastic thin shrink small outline package; 24 leads; body width 4.4 mm

**SOT355-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				-99-12-27 03-02-19

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**8-channel I<sup>2</sup>C switch with reset****PCA9548**

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**REVISION HISTORY**

Rev	Date	Description
_2	20040930	<b>Product data sheet (9397 750 14117). Supersedes data of 2002 Feb 19 (9397 750 09461).</b> Modifications: <ul style="list-style-type: none"><li>• Table 1. "Control Register; Write — Channel Selection / Read — Channel Status" on page 4: add 'No channel selected ; power-up/reset default state' row to bottom of table.</li></ul>
_1	20020219	<b>Product data (9397 750 09461). ECN 853-2318 27757 of 19 February 2002.</b>

8-channel I<sup>2</sup>C switch with reset

PCA9548



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> [3]	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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